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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/035,247	01/04/2002	Sang Hyun Yi	262/009	2931

7590 11/10/2003

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 11/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	10/035,247	YI ET AL.	
	Examin r	Art Unit	
	Christian Wilson	2824	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *18-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1 – 17 in Paper No. 6 is acknowledged.

2. Claims 18 – 28 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa in view of Matsukawa.

Regarding claim 1, Ozawa (US 4,467,345) teaches a semiconductor device [Figure 4A] comprising a plurality of metal line patterns **8** having a predetermined surface area where two adjacent metal line patterns are spaced apart from each other at a predetermined distance. Ozawa teaches a distance of 10 μm between the metal line patterns. Matsukawa (US 4,835,591) teaches a semiconductor device with metal line patterns that are less than 10 μm apart [column 5, lines 5-9]. It would have been obvious to one of ordinary skill in the art to space the metal line patterns of Ozawa less than 10 μm apart since this provides a high integration density as taught by Matsukawa [column 2, lines 30-36].

Regarding claims 2 and 3, Ozawa further teaches that the distance is greater than 1.0 μm and 1.5 μm [column 4, line 25].

Regarding claim 4, Ozawa further teaches that the area is greater than 30 μm by 30 μm [column 4, lines 25-28].

Regarding claim 5, Ozawa teaches a semiconductor device [Figure 4A] comprising a metal line layer [Figure 4B] with a plurality of metal line patterns **8** spaced apart from each other and an underlying layer **6** under the metal line layer. Ozawa teaches a distance of 10 μm between the metal line patterns. Matsukawa teaches a semiconductor device with metal line patterns that are less than 10 μm apart [column 5, lines 5-9]. It would have been obvious to one of ordinary skill in the art to space the metal line patterns of Ozawa less than 10 μm apart since this provides a high integration density as taught by Matsukawa [column 2, lines 30-36]. In response to applicant's claim that the spacing is sufficient to prevent a crack from occurring in the underlying layer, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). Since there is no difference between the claimed structure and the device in Ozawa, the claimed intended use does not patentably distinguish the claimed invention from the prior art. Further, Ozawa anticipates the use of the disclosed invention to prevent crack formation [column 2, lines 20-25, 53-55].

Regarding claims 6 and 7, Ozawa further teaches that the distance is greater than 1.0 μm and 1.5 μm [column 4, line 25].

Regarding claim 8, Ozawa further teaches an underlying insulating layer [column 3,line 52].

Regarding claim 9, Ozawa further teaches that the area is greater than 30 μm by 30 μm [column 4, lines 25-28].

5. Claims 10 – 17, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozawa in view of Matsukawa and Hara *et al.*

Regarding claim 10, Ozawa teaches a semiconductor device [Figure 4A] comprising a plurality of metal line patterns **8** where two adjacent metal line patterns are spaced apart from each other. Ozawa teaches a distance of 10 μm between the metal line patterns. Matsukawa teaches a semiconductor device with metal line patterns that are less than 10 μm apart [column 5, lines 5-9]. It would have been obvious to one of ordinary skill in the art to space the metal line patterns of Ozawa less than 10 μm apart since this provides a high integration density as taught by Matsukawa [column 2, lines 30-36]. Hara *et al.* (US 5,229,642) teaches a semiconductor device [Figure 5] where in an adjacent metal line pattern, one pattern has a slit **13**. It would have been obvious to one of ordinary skill in the art to combine the metal slit of Hara *et al.* with the metal line pattern of Ozawa and Matsukawa since the slit reduces the effective width of the line and prevents cracks [column 2, lines 41-45].

Regarding claim 11, Hara *et al.* further teaches a slit with a width greater than 1.0 μm [column 5, lines 1-5]. It would have been obvious to one of ordinary skill in the art to use a slit with a width greater than 1.0 μm since this width prevents the increase of the resistance of the metal line.

Regarding claim 12, Hara *et al.* further teaches a slit formed at a predetermined distance from the edge of the metal line pattern [Figure 5]. It would have been obvious to one of ordinary skill in the art to form the slit at a distance from the edge of the pattern since this reduces the stress in the metal line layer and eliminates cracks [column 5, lines 20-25].

Regarding claim 14, Ozawa teaches a semiconductor device [Figure 4A] comprising a metal line layer [Figure 4B] with a plurality of metal line patterns **8** spaced apart from each other and an underlying layer **6** under the metal line layer. Ozawa teaches a distance of 10 μm between the metal line patterns. Matsukawa teaches a semiconductor device with metal line patterns that are less than 10 μm apart [column 5, lines 5-9]. It would have been obvious to one of ordinary skill in the art to space the metal line patterns of Ozawa less than 10 μm apart since this provides a high integration density as taught by Matsukawa [column 2, lines 30-36]. Hara *et al.* teaches a semiconductor device [Figure 5] where in an adjacent metal line pattern, one pattern has a slit **13**. It would have been obvious to one of ordinary skill in the art to combine the metal slit of Hara *et al.* with the metal line pattern of Ozawa and Matsukawa since the slit reduces the effective width of the line and prevents cracks [column 2, lines 41-45].

Regarding claims 15 and 16, Hara *et al.* further teaches a slit parallel to the space between the adjacent metal line patterns with a width greater than 1.0 μm [column 5, lines 1-5]. It would have been obvious to one of ordinary skill in the art to use a slit with a width greater than 1.0 μm parallel to the space between the adjacent metal line patterns since this configuration prevents the increase of the resistance of the metal line and eliminates cracks.

Regarding claims 13 and 17, Ozawa and Matsukawa as modified by Hara *et al.* teach the limitations of claims 12 and 14 as described above. Matsukawa teaches a slit in an adjacent metal line pattern which is spaced less than 4 μm from the edge of the metal line pattern [column 4, line 66]. It would have been obvious to one of ordinary skill in the art to use this distance for the metal slit of Hara *et al.* in the device of Ozawa since this distance prevents the formation of hillocks on the metal line [column 4, lines 67-68].

Regarding claim 29, Ozawa teaches a semiconductor device [Figure 4A] comprising a plurality of metal line patterns **8** where two adjacent metal line patterns are spaced apart from

each other. Ozawa teaches a distance of 10 μm between the metal line patterns. Matsukawa teaches a semiconductor device with metal line patterns that are less than 2 μm apart [column 5, lines 5-9]. Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). It would have been obvious to one of ordinary skill in the art to space the metal line patterns of Ozawa less than 1.5 μm apart since this provides a high integration density as taught by Matsukawa [column 2, lines 30-36] and the distance between the metal line patterns is shown by Matsukawa to be a result-effective variable which could be optimized by routine experimentation. Hara *et al.* teaches a semiconductor device [Figure 5] where in an adjacent metal line pattern, one pattern has a slit **13**. It would have been obvious to one of ordinary skill in the art to combine the metal slit of Hara *et al.* with the metal line pattern of Ozawa and Matsukawa since the slit reduces the effective width of the line and prevents cracks [column 2, lines 41-45].

Regarding claim 30, Ozawa teaches a semiconductor device [Figure 4A] comprising a metal line layer [Figure 4B] with a plurality of metal line patterns **8** spaced apart from each other and an underlying layer **6** under the metal line layer. Hara *et al.* teaches a semiconductor device [Figure 5] where in an adjacent metal line pattern, one pattern has a slit **13**. It would have been obvious to one of ordinary skill in the art to combine the metal slit of Hara *et al.* with the metal

line pattern of Ozawa and Matsukawa since the slit reduces the effective width of the line and prevents cracks [column 2, lines 41-45]. Matsukawa further teaches a slit in an adjacent metal line pattern which is spaced less than 4 μm from the edge of the metal line pattern [column 4, line 66]. It would have been obvious to one of ordinary skill in the art to use this distance for the metal slit of Hara *et al.* in the device of Ozawa since this distance prevents the formation of hillocks on the metal line [column 4, lines 67-68].

Response to Arguments

6. Applicant's arguments with respect to claims 1 – 17 have been considered but are moot in view of the new grounds of rejection.

Conclusion

7. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (703) 308-6265. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0658.

Christian Wilson, Ph.D.
Patent Examiner
Art Unit 2824

CDW
November 3, 2003

VANTHU NGUYEN
PATENT EXAMINER